IN THE CLAIMS

1. (Currently Amended) A semiconductor IC (integrated circuit) chip, ~~A structure for a bond pad used on a semiconductor device~~ A semiconductor IC (integrated circuit) chip, comprising:

a metal line ~~layer~~;

an interconnect formed through a dielectric layer connecting to the metal line ~~layer~~;

a bond pad having a first portion disposed over the metal line ~~layer~~ and the interconnect, and a second portion disposed over the dielectric layer and offset from the metal line;

the first portion including a bond area for providing an attachment point for a connection; and

the second portion including a probe area for providing contact with a probe, wherein the bond area is separate from the probe area.

2. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 1, wherein the metal line ~~layer~~ includes copper.

3. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 1, wherein the bond pad includes aluminum.

4. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 1, further comprising a barrier layer disposed between the interconnect and the metal line ~~layer~~ to prevent diffusion therebetween.

5. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 1, wherein the bond pad includes a thickness of less than about 2 microns.

6. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 1, further comprising a passivation layer formed on at least a portion of the bond pad to protect the bond pad.

7. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 6, wherein the passivation layer includes a first opening for the bond area and a second opening for the probe area.

8. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 6, wherein the passivation layer includes an opening shared by the bond area and the probe area.

9. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 1, wherein the bond pad is permanently connected to a bond wire.

10. (Currently Amended) ~~A structure for a bond pad used on a semiconductor device~~ A semiconductor IC (integrated circuit) chip, comprising:

a metal layer patterned to form at least one metal line;

a dielectric layer formed on the metal layer and patterned to form a via to the at least one metal line;

a barrier layer formed in contact with the at least one metal line ~~layer~~ through the via;

an interconnect formed in the via and connecting to the at least one metal line ~~layer~~ through the barrier layer;

a bond pad having a first portion disposed over the at least one metal line ~~layer~~ and the interconnect, and a second portion disposed over the dielectric layer and offset from the at least one metal line;

the second ~~first~~ portion including a probe area for providing contact with a probe for device testing; and

the first ~~second~~ portion including a bond area for providing an attachment point for a bond wire, wherein the bond area is separate from the probe area.

11. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 10, wherein the metal layer includes copper.

12. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 10, wherein the bond pad includes aluminum.

13. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 10, wherein the barrier layer includes Ta or TaN.

14. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 10, wherein the bond pad includes a thickness of less than about 2 microns.

15. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 10, further comprising a passivation layer formed on the bond pad.

16. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 15, wherein the passivation layer includes a first opening for the bond area and a second opening for the probe area.

17. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 15, wherein the passivation layer includes an opening shared by the bond area and the probe area.

18. (Currently Amended) ~~A structure for a bond pad used on a semiconductor device~~ A semiconductor IC (integrated circuit) chip, comprising:

a copper layer patterned to form at least one metal line;

a dielectric layer formed on the copper layer and patterned to form a via to the at least one metal line;

a diffusion barrier layer formed in contact with the at least one metal line ~~copper layer~~ through the via;

an aluminum interconnect formed in the via and connecting to the at least one metal line ~~metal layer~~ through the diffusion barrier layer, the diffusion barrier layer for preventing atomic mixing between the at least one metal line ~~copper layer~~ and the aluminum interconnect;

a bond pad integrally formed with the interconnect and having a first portion disposed over the at least one metal line ~~metal layer~~ and the interconnect, and a second portion disposed over the dielectric layer and offset from the at least one metal line;

the second ~~first~~ portion including a probe area for providing contact with a probe for testing the semiconductor IC chip ~~device testing such that probing the probe area eliminates the capability for damage to the diffusion barrier layer and the second portion~~; and

the first ~~second~~ portion including a bond area for providing an attachment point for a bond wire, wherein the bond area is separate from the probe area.

19. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 18, wherein the barrier layer includes Ta or TaN.

20. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 18, wherein the bond pad includes a thickness of less than about 2 microns.

21. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 18, further comprising a passivation layer formed on the bond pad.

22. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 21, wherein the passivation layer includes a first opening for the bond area and a second opening for the probe area.

23. (Currently Amended) The semiconductor IC chip ~~structure~~ as recited in claim 21, wherein the passivation layer includes an opening shared by the bond area and the probe area.